

AMENDMENTS TO THE CLAIMS

1-21. (Cancelled)

22. (Original) A magnetic random access memory structure comprising:

a plurality of longitudinally extending planarized conductive lines formed over an insulating layer of a semiconductor substrate;

respective first magnetic layers over said conductive lines;

respective second magnetic layers over said first magnetic layers;

at least one contact; and

a planarized conductive material layer formed between said planarized conductive lines and said first magnetic layers.

23. (Original) The structure of claim 22 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

24. (Original) The structure of claim 22 wherein said material layer is a resistive material.

25. (Original) The structure of claim 22 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO₂, Si₃N₄ and polyimide.

26. (Original) The structure of claim 22 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

27. (Original) The structure of claim 22 wherein said conductive lines are formed in a trench formed in said substrate.

28. (Original) A memory device comprising:
at least one magnetic random access memory cell, said magnetic random access memory cell comprising a first ferromagnetic layer formed over a first planarized conductor, a second ferromagnetic layer formed over said first ferromagnetic layer, a nonmagnetic layer between said first and second ferromagnetic layers, and a planarized conductor layer provided between said first conductor and said first ferromagnetic layer.

29. (Original) The device of claim 28 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

30. (Original) The device of claim 28 wherein said material layer is a resistive material.

31. (Original) The device of claim 28 wherein said insulating layer is selected from the group consisting of BPSG, SiO₂, Si₃N₄ or polyimide.

32. (Original) The device of claim 28 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

33. (Original) The device of claim 28 wherein said first conductor is formed in a trench of a substrate.

34. (Original) A processor-based system, comprising:
a processor; and

an integrated circuit coupled to said processor, said integrated circuit including a plurality of magnetic random access memory cells, each of said magnetic random access memory cells including a first ferromagnetic layer formed over a first planarized conductor, a second ferromagnetic layer formed over said first ferromagnetic layer, a nonmagnetic layer between said first and second ferromagnetic layers, and a planarized conductor layer provided between said first conductor and said first ferromagnetic layer.

35. (Original) The system of claim 34 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

36. (Original) The system of claim 34 wherein said material layer is a resistive material.

37. (Original) The system of claim 34 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO₂, Si₃N₄ and polyimide.

38. (Original) The system of claim 34 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

39. (Original) The system of claim 34 wherein said first conductor is formed in a trench of a substrate.